AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. ~~(Original)~~ (Currently Amended) Apparatus for processing data, said apparatus comprising:

~~at least one memory~~ a plurality of memories, each having a plurality of memory storage locations associated with respective memory addresses;

a self-test controller operable to control self-test of said plurality of memories ~~at least one memory~~ including generating physical memory address signals; and

a mapping circuit for each of said plurality of memories, said mapping circuit being operable to map said physical memory address signals generated by said self-test controller to corresponding logical address signals for use by ~~said at least one memory~~ a respective one of said plurality of memories to perform a memory test based upon a physical position of memory storage locations; and

a processor core,

wherein said processor core, said at least one memory and said self-test controller are formed together on an integrated circuit~~.~~, and

wherein said mapping circuit is part of an interface circuit disposed between said self-test controller and said corresponding memory, said interface circuit being operable to adapt values and timings of signals passed between said self-test controller and said

respective one of said plurality of memories to accommodate differing value and timing properties of said respective one of said plurality of memories.

2. (Original) Apparatus as claimed in claim 1, wherein said physical memory address signals include row address signals and column address signals for addressing a memory having a row and column layout.

3. (Original) Apparatus as claimed in claim 1, wherein said mapping circuit is operable to map first physical memory address signals addressing a first memory location and second physical memory address signals addressing a second memory location to first logical address signals addressing said first memory location and second logical address signals addressing said second memory location respectively such that a memory test being performed by said self-test controller and based upon relative physical position of said first memory location and said second memory location still operates when said at least one memory is addressed with said logical address signals.

4. ~~(Currently Amended)~~ (Previously Presented) Apparatus as claimed in claim 1, wherein said at least one memory is a synthesized memory or a custom memory.

5. (Canceled).

6. (Canceled).

7. (Original) Apparatus as claimed in claim 1, comprising a plurality of memories, a mapping circuit being provided for each of said memories.

8. (Currently Amended) A method of testing a plurality of memories ~~memory~~ of a data processing apparatus having a processor core, each of said plurality of memories

~~said memory~~ having a plurality of memory storage locations associated with respective memory addresses, said method comprising the steps of:

generating physical memory address signals using a self-test controller; and

mapping, for each of said plurality of memories being tested, said physical memory address signals to corresponding logical address signals for use by a respective one of said plurality of memories ~~said memory~~ to perform a memory test based upon a physical position of memory storage locations,

wherein the processor core, said plurality of memories ~~memory~~, and said self-test controller are formed together on an integrated circuit~~.~~, and

wherein values and timings of signals passed to each of said plurality of memories are adapted to accommodate differing value and timing properties of the respective one of said plurality of memories.

9. (Original) A method as claimed in claim 8, wherein said physical memory address signals include row address signals and column address signals for addressing a memory having a row and column layout.

10. (Original) A method as claimed in claim 8, wherein first physical memory address signals addressing a first memory location and second physical memory address signals addressing a second memory location are mapped to first logical address signals addressing said first memory location and second logical address signals addressing said second memory location respectively such that a memory test being performed based upon relative physical position of said first memory location and said second memory

location still operates when said at least one memory is addressed with said logical address signals.

11. ~~(Currently Amended)~~ (Previously Presented) A method as claimed in claim 8, wherein said memory is a synthesized memory or a custom memory.

12. (Canceled).

13. (Canceled).

14. (Canceled).